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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/500,254	02/08/2000	Hans Jurgen Mattausch	4853-000001	2313

826 7590 02/27/2003

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EXAMINER

PORTKA, GARY J

ART UNIT	PAPER NUMBER
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2188

21

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/500,254

Applicant(s)  
Mattausch

Examiner  
Gary J. Portka

Art Unit  
2188



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Nov 25, 2002
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☒ Interview Summary (PTO-413) Paper No(s). 21
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 20 6) ☐ Other:

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***DETAILED ACTION***

***Continued Prosecution Application***

1. The request filed on November 12, 2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/500,254 is acceptable and a CPA has been established. An action on the CPA follows.

Claim 1 has been amended, and claim 6 has been added by Applicant. Claims 1-6 are pending.

***Information Disclosure Statement***

2. The information disclosures submitted December 2, 2002 (paper no. 20) was considered.

***Claim Objections***

3. The disclosure is objected to because of the following informalities:

a. Claim 6 does not appear to further limit claim 1.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Claims 1, 3/1, and 6 are rejected under 35 U.S.C. 103(a) as obvious over Heugel et al., U.S. Patent 5,495,570 (hereinafter "Heugel"), in view of DeWilde et al., U.S. Patent 6,434,674 B1 (hereinafter "DeWilde").

6. As to claims 1 and 6, Heugel discloses the recited shared memory comprising: plurality of multiport memories (20, Figure 2) accessible from a copybus side (26A, 26B) and a user side (23), at least one copybus (26A, 26B), the shared memory adapted to copy contents of one of the memories which has been changed by writing from the user side, to other memories through the copybus (see Abstract, Figures 1 and 2, column 4 lines 5-13, column 5 lines 12-40, and column 7 lines 17-25).

Heugel does not teach that the multiple port memories provide internally concurrent access (the meaning intended by the claim language, clarified by Applicant's arguments, but see Response to Arguments below). However, the advantages of multiple port memory having internally concurrent access were well known, and taught by DeWilde at column 1 lines 29-52. DeWilde teaches a true multiport memory implementation provides internally concurrent random accesses for each port, removes initial access time penalty, and is an inherently simple design because multiplexors are not required. From these teachings, an artisan would have recognized that these advantages could be achieved in the multiport memory of Heugel by implementing it in this way, and thus would have been motivated to do so. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use in Heugel a multiport memory providing internally concurrent access, because as taught by DeWilde such a true multiport memory provides internally

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concurrent random accesses, removes initial access time penalty, and avoids the requirement to add multiplexors.

7. As to claim 3/1, Heugel discloses the memories are formed by an integrated circuit technique (since RAM 20 is considered as formed by an integrated circuit technique).

8. Claims 2, 3/2, and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heugel in view of DeWilde, and further in view of Hirose, JP Patent 61-3450 (A) (hereinafter "Hirose").

9. As to claims 2, 3/2, and 5, neither Heugel nor DeWilde disclose copying optically. However, the technique was well known in the art and was taught by Hirose. The device of Hirose is taught to improve signal transmission speed in a shared memory, and clearly invokes the trend of reducing cost and improving performance by increasing integration as compared to the other references. The device is formed by a three dimensional integrated circuit technique. Thus it would have been obvious to one of ordinary skill in the art to copy optically with a three dimensional integrated circuit device, because such a device and method was previously taught by Hirose as improving performance.

10. As to claim 4, while Hirose teaches a three dimensional integrated device, an artisan would have known that older two dimensional devices were still applicable, and would have desired such a device for the purposes of reducing cost, or for compatibility with existing manufacturing facilities and/or interfacing circuits. Thus it would have been obvious to use a two dimensional integrated circuit technique, because this is well known as a cheaper manufacturing alternative, and may improve compatibility requirements.

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***Response to Arguments***

11. Applicant's arguments filed November 25, 2002 have been fully considered but they are moot in view of the new grounds of rejection.

Applicants argue that a "shared memory" is defined in the art as supplying an identical database to multiple users. Although the rejection was changed, Examiner nonetheless disagrees with the statement in general. Unless the present specification defines otherwise, a "shared memory" may be reasonable interpreted as simply any memory that may be accessed or shared by more than one requestor.

Applicants argue that true multiport memory is required to provide the recited "internally concurrent access". Although the rejection was changed, Examiner disagrees with the statement to the extent that it is supported by the claim language. For example, Examiner contends that even the single port array with multiplexing scheme taught by DeWilde as one type of multiport memory (as cited hereinabove) may be considered to have internally concurrent access by considering the multiplexor(s) to be internal to the memory. However, in the interest of expediting prosecution, Examiner has interpreted the claim language hereinabove as previously argued by Applicant. It is suggested to amend this language to prevent the broad interpretation offered above.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No.

6,480,927 B1    Modular memory with multiple ports having simultaneous access.

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13. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in Abandonment of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

14. Any inquiry concerning this communication from the examiner should be directed to Gary J. Portka at telephone number (703) 305-4033. The examiner can normally be reached on weekdays from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached at (703) 308-4908.

Any response to this final action should be mailed to (or faxed as provided below):

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (Receptionist).

The fax phone number for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238	(After Final communications)
(703) 746-7239	(Official communications)
(703) 746-7240	(Status inquiries, draft communications)

Any inquiry of a general nature relating to this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 305-3900.

Gary J. Portka  
Primary Examiner  
February 20, 2003

